METHOD OF FABRICATING SEMICONDUCTOR DEVICES HAVING DEEP AND SHALLOW ISOLATION STRUCTURES

BACKGROUND OF THE INVENTION

This invention relates, in general, to semiconductor devices, and more particularly to a method of fabricating a semiconductor structure that is compatible with multiple technologies.

In the semiconductor art, a trend is toward the fabrication of device structures that are compatible with multiple technologies. For example, structures allowing for the implementation of both bipolar and MOS devices in a single integrated circuit are highly desirable because the best characteristics of both technologies may be obtained. This allows for the fabrication of CMOS and BIMOS high performance integrated circuits. For fabrication methods of multiple technology integrated circuits to become practical, process integration flexibility must be obtained. Additionally, it is desirable to be able to develop methods of fabrication having enhanced scalability characteristics.

Prior art methods of fabricating semiconductor structures having variable width shallow isolation elements, especially those disposed over deep trench isolation elements generally require multiple masking steps. Specifically, masks are used to define the encroachment of the isolation elements into the active regions. Inherent with multiple masking steps are misalignment tolerances that must be provided for. These misalignment tolerances prohibit aggressive scaling of structures and require additional real estate.

In view of the above, it would be highly desirable to have a method of fabricating semiconductor structures having variable width shallow isolation elements self-aligned to deep trench isolation elements.

SUMMARY OF THE INVENTION

Accordingly, it is an object of the present invention to provide a method of fabricating a semiconductor structure that is compatible with several technologies.

One more object of the present invention is to provide a method of fabricating a semiconductor structure having increased integration flexibility.

Another object of the present invention is to provide a method of fabricating a semiconductor structure having enhanced scalability characteristics.

It is an additional object of the present invention to provide a method of fabricating a semiconductor structure wherein both deep trench isolation elements and shallow dielectric isolation elements may be fabricated at variable widths.

Yet a further object of the present invention is to provide a method of fabricating a semiconductor structure that may be employed in conjunction with high performance integrated circuits.

The foregoing and other objects and advantages are achieved in the present invention by one embodiment in which, as a part thereof, includes providing a semiconductor substrate and forming a thermal oxide layer, a polysilicon layer and a first dielectric layer thereon. A first mask is formed on the first dielectric layer and is used to form at least one opening therein that extends to the polysilicon layer. Dielectric spacers are then formed in the opening to allow for a self-aligned reduction in width of a trench formed in the substrate beneath the opening. After forming a dielectric trench liner in the trench, the trench is filled and the dielectric spacers can be removed to expose the portions of the polysilicon layer disposed beneath. The removal of the dielectric spacers creates a self-aligned offset between the trench liner and the edge of the first dielectric layer which will serve as a mask for the formation of shallow dielectric isolation elements. A second mask is then employed and allows for the selective removal of the first dielectric layer in areas where it was not earlier removed during the formation of the openings. Shallow isolation elements are then formed in the areas where the first dielectric layer has been removed.

A more complete understanding of the present invention can be attained by considering the following detailed description in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIGS. **1–16** are highly enlarged cross-sectional views of a portion of a semiconductor structure during processing; and

FIGS. **17–18** are highly enlarged cross-sectional views of a portion of a semiconductor structure prior to active device formation.

DETAILED DESCRIPTION OF THE INVENTION

FIGS. **1–16** are highly enlarged cross-sectional views of a portion of a semiconductor structure during processing. It should be understood that the figures herein may not be precisely to scale. Initially, a substrate **10** is provided. In this embodiment, substrate **10** is comprised of monocrystalline silicon however it should be understood that substrates comprising other materials may be used. Depending upon the device application, substrate **10** may comprise semiconductor material wherein pre-isolation processing has been completed to establish required doping profiles and epitaxial layers. A thin thermal oxide layer **12** is formed on substrate **10** followed by the formation of a thin polysilicon layer **14** thereon, preferably by deposition. As one skilled in the art will understand, polysilicon layer **14** will serve as a buffer for the local oxidation which will be explained presently. A nitride layer **16** is formed on polysilicon layer **14**. Nitride layer **16** is formed by CVD in this embodiment although other well known methods may be employed. An oxide layer **18** is then formed, preferably by CVD, on nitride layer **16**.

Following the formation of oxide layer **18**, a photoresist mask **20** is formed thereon. The formation of photoresist mask **20** includes patterning a photoresist layer by methods well known in the art. Mask **20** is employed to form openings **22** that extend through oxide layer **18** and nitride layer **16** and stop on polysilicon layer **14** as shown in FIG. **2**. Openings **22** are formed by reactive ion etching. Once openings **22** have been formed, photoresist mask **20** is removed by a standard photoresist clean.

As shown in FIG. **3**, dielectric spacers **24** are formed in openings **22**. Spacers **24** are comprised of oxide in this embodiment although nitride or oxynitride may be employed. Oxide spacers **24** are formed by depositing, either by CVD or PECVD, an oxide layer (not shown) and then reactive ion etching the oxide layer to form oxide spacers **24**. It should be understood that this oxide spacer etch stops on polysilicon layer **14**. Spacers **24** allow for a self-aligned reduction in the widths of open-